Absorption Enhancing and Passivating Non-planar Thin-Film Device Architectures for Copper Indium Gallium Selenide Photovoltaics

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***Abstract* — The sub-micrometer absorber regime is currently being explored to reduce materials usage and deposition time while simultaneously increasing device voltages due to increased generated carrier concentration. In order to realize these benefits, the absorption of photons must be maintained or even increased while avoiding detrimental recombination. Reported here are optoelectronic simulations that highlight photon and generated carrier management opportunities for improvement of thin film Cu(InxGa1-x)Se2 (CIGSe) device performance. Structures that could be created via either self-assembly, patterning by nanoimprint lithography, or a combination of both are predicted to significantly increase short circuit current density and open circuit voltage simultaneously.**

***Index Terms* — light trapping, nanopatterning, nanophotonics, solar energy, photovoltaic cells, thin film devices .**

I. Introduction

Light trapping by use of random texture or order nanostructures has been widely demonstrated for crystalline silicon, amorphous silicon, and GaAs photovoltaics [1]–[5], but these approaches have not been as extensively applied to polycrystalline thin-film compound materials and photovoltaic devices, such as CIGSe, CdTe, and Cu_2ZnSnS_4.[6], [7] In this paper, we apply light management approaches to CIGSe photovoltaic device design and demonstrate opportunities for improvement to both the short-circuit current density (JSC) and open circuit voltage (VOC) via optoelectronic simulations.

The benefits of decreasing the thickness of CIGSe absorber layers range from the practical materials, deposition time, and cost savings to the physical enhancement of the open-circuit voltage via the spatial confinement of generated carriers and a reduced probability of bulk recombination of carriers generated far from the junction. At these injection levels, thinner absorbers exhibit greater quasi-fermi level splitting, however the voltage gains are typically offset by increased recombination at the junction and back-contact interface. [8] Thus, in studying structured devices, accurate modeling of the spatial distribution of generated carriers is important.

Only a full optoelectronic model, such as the one used herein, can quantitatively relate optical absorption enhancement and electronic transport. It can also highlight electronic transport issues which can be overcome by improved design.[9] For example, we report that randomly textured CIGSe absorbers absorbs the majority of incident photons in a film of 700 nm planar equivalent thickness (t_{EQ}), but generated carriers are lost to parasitic recombination in near the back contact interface. We also show similar performance is possible from a properly designed periodic 2-dimensional dielectric grating with a 800nm t_{EQ}. Here we identify possible CIGSe device architectures that enable thinning of the CIGSe less than one micrometer while maintaining or improving the J_{SC} and/or the V_{OC} compared to those of thicker planar devices.

II. Methods

Cross-sectional images of unique, randomly textured CIGSe thin film photovoltaic absorbers were obtained from the Heliovolt Corporation while the company was still active in Research and Development efforts. Using these images, optoelectronic simulations aimed to identify mechanisms of light trapping to elucidate initial experimental results.[10] A representative cross-sectional image of these randomly textured microstructures can be seen in Fig. 1a, which is a CIGSe film with equivalent planar thickness of 1.7 μm. The device schematic in Fig. 1b illustrates a simulated device structure that utilizes this film morphology. It includes a 50 nm CdS conformal window layer, simulating results from conformal bath deposition. The CdS layer is coated with a 150 nm aluminum-doped zinc oxide (AZO) serves as a transparent front contact. The back contact consists of a 500 nm molybdenum (Mo) planar thin film. Fig. 1c demonstrates 1b with the addition of a dielectric separation layer with point contacts spaced on the order of the majority carrier diffusion length. Fig. 1d demonstrates a short-period grating structure superimposed on a dielectric separation layer with point contacts which can act as a photonic structure in the CIGSe

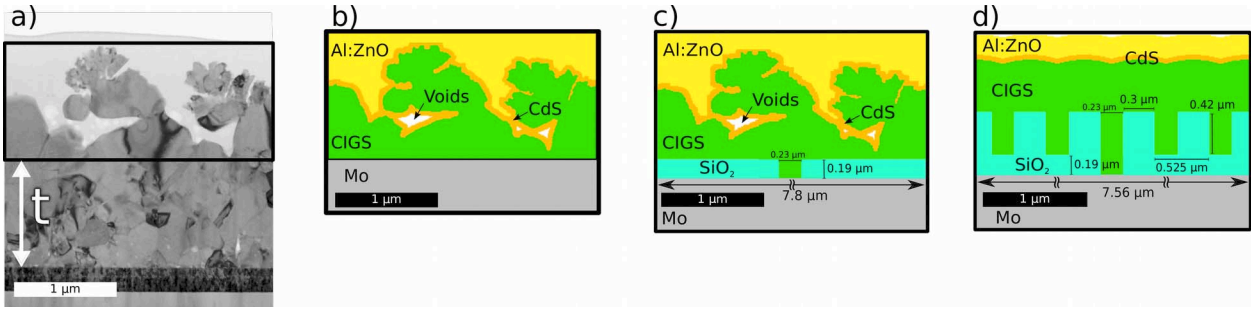

Fig 1: Simulated Cross-Sections: a) A representative focused ion beam (FIB) cross section of randomly textured CIGSe absorber films is used to define the photovoltaic model, shown in b). In c), a SiO_2 layer serves to increase reflection and define electrical contacts.

absorber. Such a structure could readily be fabricated by nanoimprint lithography.[7], [11] A conformal deposition of CIGSe is subsequently simulated as shown.

Two dimensional electromagnetic simulations using the finite-difference time-domain (FDTD) method were performed with normally incident plane wave illumination. [12] The spatial generation rate was obtained as the polarization averaged volumetric power absorption for the cross-sections 1b-1d, planar device ,and structures without the dielectric point-contact layer (not shown), power-weighted by the spectral irradiance of the ASTM -AM1.5G solar spectrum. [11] Refractive index data for fractional gallium composition close to x=0.4 was used.[13] These optical generation profiles were used as inputs to carrier transport simulations using Synopsis Sentaurus Device to calculate the steady state EQE and current density-voltage (J-V) characteristics of each device. We utilized previously reported electronic parameters for CIGSe photovoltaics of Gloeckler et.al.,[14] except where explicitly stated herein.

As an extension of results obtained in 2-dimensional simulations, the periodic grating structure was also simulate din 3-dimensions. This could no be done for the cross-sections of the randomly textured absorber however.

III. Results

The spatial generation map from FDTD simulations of Fig. 1b showed two things: (1) photo-carrier generation hot-spots in the CIGSe absorber, and (2) areas of parasitic absorption in surrounding layers. Areas of high carrier generation are generally close to the randomly textured CdS|CIGSe film interface due to the undulation of the junction. The randomly textured CIGSe surface layer absorbs most of the incident light, suggesting that the underlying CIGSe film beneath the surface topology in Fig. 1a is superfluous with respect to light absorption. Table 1, shows how the J_{SC} is relatively constant for various underlying thicknesses of planar CIGSe, referred to as t in Fig. 1a. As much as 97% of the short circuit current is maintained for an underlying thickness t=0, with the t_{EQ} of the CIGSe material is 700nm for this random morphology. This is an important result from a materials savings perspective. The photocurrent that is lost due to thinning is due to the low reflectance of the CIGSe|Mo interface leading photons lost by absorption in the Mo. This is addressed later in this study by the addition of an optimized dielectric separation layer.

Table 1 also shows the effects of thinning the device from t=1000nm to t=0nm on the V_{OC}. The voltage of the thinner device is significantly reduced due to greater generation within a diffusion length of the back contact. The simulations here assumed that the surface recombination velocity at this interface was the thermal velocity, such that all carriers that reach the back contact recombine. The simulated IQE also falls off as absorption occurs deeper in the absorber layer. This conclusion is also supported by the observed rapid increase in voltage as the generation is spatial separated from the back contact for t=200nm and only marginal amounts for subsequent thickness increases. These randomly textured devices simulated outperform their traditional t_{EQ} devices also shown in Table 1.

As an alternative to random texture, periodic grating dielectrics can give a controllable and designed texture via conformal deposition onto a dielectric nanostructure. A periodic nanostructure was optimized by varying the period, width, and height of the grating shown in 1d. The optimum was found to be a width of 300 nm, a period of 525 nm, and a height of 420 nm. Initially, the grating architecture is simulated without the 190 nm dielectric layer shown in 1d. Periodic structure, again, has a t_{EQ} of 700 nm CIGSe absorber. The JV results are listed in Table 1. The simulated J_{SC} is larger than both planar cases, but the light-trapping effect is not as strong as the textured case. However, the V_{OC} is the largest of all the devices, including larger than the thicker 1700 nm planar cell. This can be attributed to multiple simultaneous factors. First, more minority carriers are being generated in a smaller area, driving the quasi-fermi levels further apart in energy compared to thicker devices. Second, the leading interface of the absorber|window layer, where the majority of generation occurs, is spatially separated from the back contact by nearly a micron due to the area that is taken by the grating. Lastly, the interfacial area of the absorber that is in contact with the back-contact is reduced due to masking by the

TABLE I

JV Characteristics of Different CIGSe Architectures

Simulated Device	V_{OC} (mV)	J_{SC} (mA/cm^2)	Fill Factor (%)	Efficiency (%)
Texture, t = 0 nm	605.3	-34.3	77.8	16.1
Texture, t = 200 nm	621.7	-34.6	78.9	17.0
Texture, t = 400 nm	628.0	-34.8	79.0	17.3
Texture, t = 600 nm	631.3	-35.0	79.1	17.5
Texture, t = 800 nm	633.1	-35.0	79.1	17.5
Texture, t = 1000 nm	634.2	-35.1	79.1	17.6
Planar t = 700 nm	625.2	-31.8	77.4	15.4
Planar t = 1700 nm	637.8	-33.0	78.0	16.5
Periodic t_{eq} =700nm	640.1	-33.6	78.5	16.9

dielectric.[7] Here, the surface recombination velocity at the dielectric|CIGSe interface is a forgiving value of 10^3 cm/s, and this voltage loss pathway is minimal.

The voltage boost seen in the periodically textured absorber gives insight as to how to further gain efficiencies in the random texture and planar architectures. In order to combat the losses in these devices, planar dielectric separation layers at the CIGSe|Mo interface were studied as a potential route to increase the reflectance at this interface, gaining double pass absorption, and as a potential opportunity to passivate the back contact interface.[15], [16] To maintain generality, these dielectric separation layers were studied in the case of planar architectures, randomly textured devices (Fig. 1c), and also periodically structured devices (Fig. 1d). It is proposed that these dielectric separation layer could be fabricated with low refractive index silica sol gel (n=1.42) and patterned via nanoimprint lithography.[17], [18] The dielectric layer is designed to reflect light back into the CIGSe absorber via destructive thin-film interference wavelengths near the band-edge, corresponding to ¼ wavelength of 1070 nm in the low index dielectric. Because of the scattering caused by the randomly textured absorber, and FDTD optimization was performed to ensure that a ¼ wavelength layer was optimum. Indeed, and dielectric layer of ~190nm gave optimal reduction in Mo parasitic absorption. The change in AM1.5-G absorbed photocurrent in the CIGSe is shown in Fig. 2 where the solid curves are with the separation layer and the dashed curves are without it. The interference condition is met between wavelengths of ~1040-1070nm and there enhanced photocurrent absorption, shown by the inset to the left. The randomly textured device also shows an increase in absorption near the band-edge, but due to the scattering of the texture, the enhancement is significantly broadened showing smaller broadband enhancement from ~900nm to the band edge. The absorption in the Mo is decreased in all devices as shown in the middle inset. The absorbed photocurrent is increased by 0.78 mA/cm^2, 0.53 mA/cm^2, 0.27 mA/cm^2 for the planar, periodic, and randomly textured devices respectively.

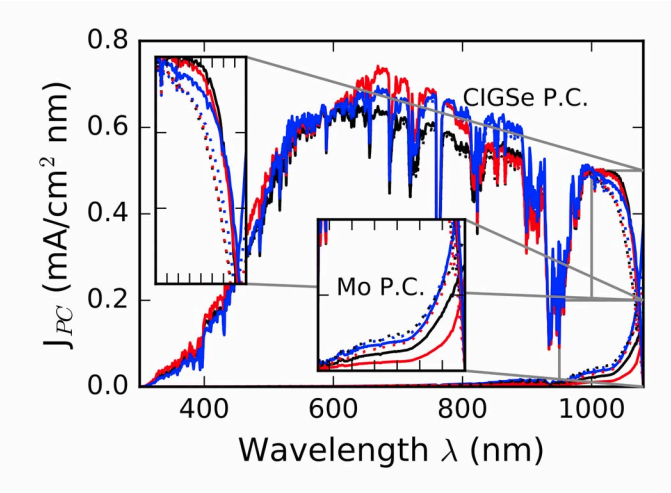

Fig 2: The absorbed photocurrent under AM1.5-G illumination of different device architectures, random (blue), periodic (red), and planar (black) are shown without (dashed curves) and with (solid curves) dielectric separation layers.

Fig. 2 also highlights the differences of enhancement wavelengths for the random and periodic architectures. The red curves of the periodic structure show peak photocurrent absorbtion between 600-700nm where the photon flux is greatest. Periodic nanostructures work best when only targeting a narrow band of wavelengths for which resonant modes can be created, thus the parameter optimization gives the architecture that couples this peak in photon flux. The absorbed photocurrent at longer wavelengths is insuffciently trapped and the absorbtion under-performs the t_{EQ} device in this range. In contrast, the random texture provides a large and broadband absorption enhancement over the planar t_{EQ} via an anti-reflection effect, rather than a resonant effect.

The thin film dielectric separation layers embedded between the CIGSe absorber and Mo contact provide a barrier to minority carrier recombination if appropriate surface passivation can be achieved at CIGSe|dielectric interfaces. Surface recombination velocities in the range of 100-10^4 cm s^{-1} have been reported for alumina dielectric layers, and similar values could be expected with other oxides such as silica.

[19] As an example, the randomly textured absorber (t=0nm) sees a boost in the V_{OC} from 605.3 mV without a dielectric layer to ~650 mV with it in this SRV range at the CIGSel dielectric interface. The simulated JV curve is shown in Fig. 3a by the the solid blue line. This led to the best performing device with an efficiency of 18.1%, which outperforms the t_{EQ} (700nm CIGSe, 15.4%) and even a thicker 3µm CIGSe device (16.4%) with the same electronic properties. Similar increases in V_{OC} were seen for both other architectures when the dielectric separation layer was implemented. These layers therefore reduce contact recombination similar to Ga grading, but have the added effect of increased reflectance. To push the device performance a bit further, a 90nm ¼ wavelength MgF_2 anti-reflection coating was applied to the front-side of the devices, shown by the dashed lines in Fig 3a. Combining this proven light trapping technique with a randomly textured CIGSe absorber and a dielectric separation layer at the back-contact, device efficiency reached over 19% for a 700 nm equivalent thickness absorber layer.

Finally, our optoelectronic simulations of periodic grating structures were extended to 3-dimensions to confirm the validity of our 2-dimensional results reported thus-far. An optical optimization for absorbed photocurrent was performed for a square lattice of cylinders along the plane of the back-contact and found dimensions very similar to that of the 2D grating. The optimal height and diameter were again, 420nm and 300nm respectively, while the optimal period of this lattice increased slightly to 600nm. Conformal deposition was simulated using Synopsys Sentaurus Process to get the conformal structure. The normalized optical generation of unit cells of this architecture with absorbers of 820nm and 1072nm t_{EQ} are shown in Fig. 3b. Interestingly, we see more optical generation in the thinner absorber layer. This is quantified by the J_{SC} shown Fig 3c of -36 mA/cm^2 and -31.9 mA/cm^2 for the thinner and thicker cells respectively. Light is more effectively coupled and confined to the thinner cell for this lattice. This nanophotonic structure *without* separation layer allows the patterned cell to perform comparably to the randomly textured absorber with a dielectric separation layer, with 18.3% and 18.1% effciencies respectively. Compared with our 2D approximation from before, a higher efficiency is seen in 3D simulations, highlighting the utility of optoelectronic modeling to determine optimal architectures.

IV. Conclusions

Structuring can lead to increased photocurrent absorption in thin sub-micron CIGSe absorbers compared to traditional planar devices. Randomly textured CIGSe significantly scatter incident light and lead to greatly enhance broadband absorption while periodic structures can be made to enhance specific wavelengths. This analysis showed that the increased junction interface was not a drawback for interface recombination velocities below 10^3 cm/s. Adding a dielectric separation layer to the back contact interface enhances

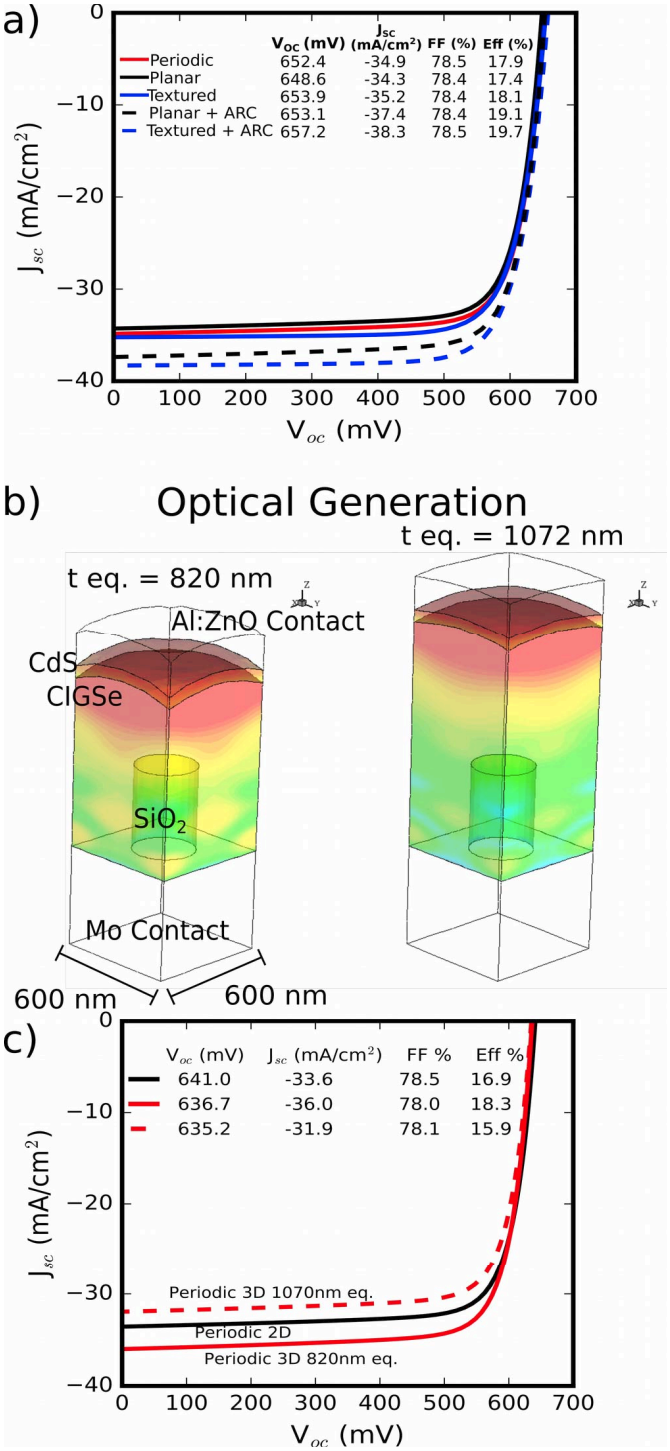

Fig 3: a) The simulated JV curves for the three architectures with the addition of a 190nm dielectric separation layer with point contacts. Also, an ARC is applied to the planar and textured devices with the dielectric layer. b) Optical generation in one unit cell of a conformally deposited CIGSe device onto a square lattice of dielectric cylinders with two different thicknesses of absorber. c) JV curves comparing the 2D model to the 3D model of the devices in b).

reflection of photons for double pass absorption with the additional opportunity for significant passivation at this interface. Combining photon and carrier management strategies such as these can lead to devices with the potential to significantly out-perform traditional planar devices. These simulation studies are supported by experimental evidence in literature, but show that greater enhancements could yet to be achieved by careful control of the CIGSe morphology, the dielectric separation layer thickness, and the point contact spacing.

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